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EXAMINER	
BONZO, BRYCE P	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/886,959	Applicant(s) AVIZIENIS, ALGIRDAS	
	Examiner Bryce P Bonzo	Art Unit 2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-66* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-48 and 52-66* is/are rejected.

7)☒ Claim(s) *49-51* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

NON-FINAL OFFICIAL ACTION

Status of the Claims

Claims 1-66 are currently pending.

Claims 1-48 and 52-65 are rejected under 35 USC 102(b).

Claims 2, 3, 7, 12, 19, 24, 27, 32-41, 54, 61, 64, 65 are rejected under 35 USC §112, second paragraph.

Claims 4, 16, 26, 36, 47, 59, 63 and 66 are rejected under 35 USC §112, fourth paragraph.

Claims 48 and 66 are objected as being duplicate claims.

Claims 49-51 are objected to while containing allowable matter.

Use of the word "substantially"

The frequent use of the word substantially throughout the claims and specification warrant a citation of the MPEP concerning the use of this word. The excerpt follows:

2173.05(b) Relative Terminology - 2100 Patentability

The term "substantially" is often used in conjunction with another term to describe a particular characteristic of the claimed invention. It is a broad term. *In re Nehrenberg*, 280 F.2d 161, 126 USPQ 383 (CCPA 1960). The court held that the limitation "to substantially increase the efficiency of the compound as a copper extractant" was definite in view of the general guidelines contained in the specification. *In re Mattison*, 509 F.2d 563, 184 USPQ 484 (CCPA 1975). The court held that the limitation "which produces substantially equal E and H plane illumination patterns" was definite because one of ordinary skill in the art would know what was meant by "substantially equal." *Andrew Corp. v. Gabriel Electronics*, 847 F.2d 819, 6 USPQ2d 2010 (Fed. Cir. 1988).

References to Documents not Provided in an IDS

The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A(1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

Objections to the Claims

Claims 48 and 66 are objected to under 37 CFR 1.75 as being a substantial duplicate of claims 43 and 63. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Rejections under 35 USC §112, second paragraph

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2, 3, 7, 12, 19, 24, 27, 32-41, 54, 61, 64, 65 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The phrase "substantially exclusively made up of substantially commercial, off-the-shelf components" is neither clear nor distinct. The use of the word substantially in patent claims is convey the concept that certain ideals infeasible are infeasible in the real world. Despite any amount of effort nothing can be truly planar or pure or round. Substantially is employed to allow for imperfections and impurities in a legal framework. In the pending claims, the computer system in question is a manmade construct, and component is placed within is deliberately included, and not a result of some real world manufacturing restriction. Further, *substantially exclusively made up of substantially* is on its surface confusing. It presents a range within a range, that is mostly exclusively made up of most commercial components. It leaves the reader asking is exclusively a valid term for this aspect of the invention as it clearly is not exclusively composed of any component. As claimed the double use of substantially causes confusion as a meaning for exclusively is not forth coming. Page 32, ¶1 in the Specification does not elaborate on this terminology to determine the precise meaning of "substantially exclusively made up of substantially commercial, off-the-shelf components."

Applicant is strongly encouraged to remove the substantially language from these claims.

Rejections under 35 USC §112, fourth paragraph

The following is a quotation of the fourth paragraph of 35 U.S.C. 112:

> Subject to the following paragraph, a claim in dependent form shall contain a reference to a claim previously set forth and then specify a further limitation of the subject matter claimed. A claim in dependent form shall be construed to incorporate by reference all the limitations of the claim to which it refers.

Claims 4, 16, 26, 36, 47, 59, 63 and 66 are rejected under 35 USC §112, fourth paragraph as they fail to further limit the scope of the claims. The *such computer system* of these claims is each case has already been claimed verbatim in the parent claim.

Rejections under 35 USC §102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-48 and 52-65 are rejected under 35 U.S.C. 102(b) as being anticipated by *The Hundred Year Spacecraft* by Algirdas Avižienis.

As per claims 1-48 and 52-65, Algirdas Avižienis discloses:

1. Apparatus for deterring failure of a computing system; said apparatus comprising:

an exclusively hardware network of components, having substantially no software (page 5, ¶1: D-nodes);

terminals of the network for connection to such system (page 5, ¶ 4 "Also COTS processor...a C-Node"); and

fabrication-preprogrammed hardware circuits of the network for guarding such system from failure (Page 5, ¶1).

2. The apparatus of claim 1, particularly for use with such system that is substantially exclusively made up of substantially commercial, off-the-shelf components; and wherein:

at least one of the network terminals is connected to receive at least one error signal generated by such system in event of incipient failure of such system (page 5, ¶1, error signal collected; and

at least one of the network terminals is connected to provide at least one recovery signal to such system upon receipt of the error signal (Page 5, ¶1: initiation of recovery sequence).

3. The apparatus of claim 2, wherein: the circuits comprise portions fabrication-preprogrammed to evaluate the at least one error signal to establish characteristics of the at least one recovery signal (Page 5, ¶1: initiates diagnosis and recovery sequences).

4. The apparatus of claim 1, further comprising: such computing system (see above).

5. The apparatus of claim 1, wherein: the circuits comprise portions for identifying failure of any of the circuits and correcting for the identified failure (page 5, ¶2).

6. The apparatus of claim 1, particularly for use with a computing system that has at least one software subsystem for conferring resistance to failure of the system and wherein (page 6, ¶5; Page 4, ¶8 "multi-version software):

the circuits comprise substantially no portion that interferes with such failure-resistance software subsystem (no interference is described).

7. The apparatus of claim 1, particularly for use with a computing system that is substantially exclusively made of substantially commercial, off-the-shelf components and that has at least one hardware subsystem for generating a response of the system to failure; and wherein (Page 5, ¶1: requires the COTS to raise the error for "error signal collection"):

the circuits comprise portions for reacting to said response of such hardware subsystem(Page 5, ¶1: "initiation of diagnosis").

8. The apparatus of claim 1, particularly for use with a computing system that has plural generally parallel computing channels (see figure 2); and wherein:

the circuits comprise portions for comparing computational results from such parallel channels (page 5, ¶2 "voting").

9. The apparatus of claim 8, wherein: the parallel channels of the computing system are of diverse design or origin (page 5, ¶4 "Diversity of hardware" applies tot eh COTS portions of the system as well as the D-nodes).

10. The apparatus of claim 1, particularly for use with a computing system that has plural processors; and wherein (figure 2): the circuits comprise portions for identifying failure of any of such processors and correcting for identified failure (page 5, ¶1 D-node).

11. The apparatus of claim 1, wherein: the circuits comprise modules for collecting and responding to data received from at least one of the terminals, said modules comprising (page 5, ¶1, D-node functionality): at least three data-collecting and -responding modules (page 5, ¶1 "two or more"), and processing sections for conferring among the modules to determine whether any of the modules has failed (page 5, ¶2 voting).

12. The apparatus of claim 1, particularly for use with a computing system that is substantially exclusively made of substantially commercial, off-the-shelf components and that has at least one subsystem for generating a response of the system to failure, and that also has at least one subsystem for receiving recovery commands (page 5, ¶1); and wherein:

the circuits comprise portions for interposing analysis and a corrective reaction between the response-generating subsystem and the command-receiving subsystem (Page 5, ¶1).

13. Apparatus for deterring failure of a computing system; said apparatus comprising:

a network of components having terminals for connection to such system (Figure 2); and

circuits of the network for operating programs to guard such system from failure (Page 5, ¶1);

the circuits comprising portions for identifying failure of any of the circuits and correcting for the identified failure (Page 5, ¶1).

14. The apparatus of claim 13, wherein: the program-operating portions comprise a section that corrects for the identified failure by taking a failed circuit out of operation (Page 5, ¶2).

15. The apparatus of claim 14, wherein: the program-operating portions comprise a section that substitutes and powers up a spare circuit for a circuit taken out of operation (page 5, ¶2: "substitute and unpowered spares" require powering up to be of use).

16. The apparatus of claim 13, further comprising: such computing system (see above).

17. The apparatus of claim 13, wherein:

the program-operating portions comprise at least three of the circuits (Page 5, ¶2 M-clusters of 3+ M-nodes); and

failure is identified at least in part by majority vote among the at least three circuits (Page 5, ¶2: voting).

18. The apparatus of claim 13, particularly for use with a computing system that has at least one software subsystem for conferring resistance to failure of the system (Page 4, ¶8,9); and wherein: the circuits comprise substantially no portion that interferes with such failure-resistance software subsystem (no such interference is disclosed).

19. The apparatus of claim 13, particularly for use with a computing system that is substantially exclusively made of substantially commercial, off-the-shelf components and that has at least one hardware subsystem for generating a response of the system to failure; and wherein (column 5, ¶1): the circuits comprise portions for reacting to said response of such hardware subsystem (page 5, ¶1).

20. The apparatus of claim 13, particularly for use with a computing system that has plural generally parallel computing channels (figure 2); and wherein: the circuits comprise portions for comparing computational results from such parallel channels (page 5, ¶2 "voting").

21. The apparatus of claim 20, wherein: the parallel channels of the computing system are of diverse design or origin (page 5, ¶2 "diverse M-nodes").

22. The apparatus of claim 13, particularly for use with a computing system that has plural processors; and wherein: the circuits comprise portions for identifying failure of any of such processors and correcting for identified failure(figure 2, pages 5 ¶2).

23. The apparatus of claim 13, wherein: the circuits comprise modules for collecting and responding to data received from at least one of the terminals, said modules comprising (Page 5, ¶1 D-nodes function): at least three data-collecting and -responding modules (page 5, ¶1: "two or more"), and processing sections for conferring among the modules to determine whether any of the modules has failed (page 5, ¶1 "voting").

24. The apparatus of claim 13, particularly for use with a computing system that is substantially exclusively made of substantially commercial, off-the-shelf components and that has at least one subsystem for generating a response of the system to failure, and that also has at least one subsystem for receiving recovery commands; and wherein (Page 5, ¶1): the circuits comprise portions for interposing analysis and a corrective reaction between the response-generating subsystem and the command-receiving subsystem (Page 5, ¶1).

25. Apparatus for deterring failure of a computing system that has at least one software subsystem for conferring resistance to failure of the system; said apparatus comprising: a network of components having terminals for connection to such system (figure 2); and circuits of the network for operating programs to guard such system from failure (page

5, ¶1); the circuits comprising substantially no portion that interferes with such failure-resistance software subsystem (page 5, ¶1).

26. The apparatus of claim 25, further comprising: such computing system, including such at least one software subsystem (see above).

27. The apparatus of claim 25, particularly for use with a computing system that is substantially exclusively made of substantially commercial, off-the-shelf components and that has at least one hardware subsystem for generating a response of the system to failure; and wherein (Page 5, ¶1): the circuits comprise portions for reacting to said response of such hardware subsystem (page 5, ¶1).

28. The apparatus of claim 25, particularly for use with a computing system that has plural generally parallel computing channels; and wherein (figure 2): the circuits comprise portions for comparing computational results from such parallel channels (page 5, ¶2 "voting").

29. The apparatus of claim 28, wherein: the parallel channels of the computing system are of diverse design or origin (page 5, ¶2"diverse M-nodes").

30. The apparatus of claim 25, particularly for use with a computing system that has plural processors; and wherein: the circuits comprise portions for identifying failure of

any of such processors and correcting for identified failure (page 5, ¶1: d-NODE functions).

31. The apparatus of claim 25, wherein: the circuits comprise modules for collecting and responding to data received from at least one of the terminals, said modules comprising (page 5, ¶1, D-node function): at least three data-collecting and -responding modules (Page 5, ¶1 two or more), and processing sections for conferring among the modules to determine whether any of the modules has failed (page 5, ¶1 voting).

32. The apparatus of claim 25, particularly for use with a computing system that is substantially exclusively made of substantially commercial, off-the-shelf components and that has at least one subsystem for generating a response of the system to failure, and that also has at least one subsystem for receiving recovery commands; and wherein (page 5, ¶1): the circuits comprise portions for interposing analysis and a corrective reaction between the response-generating subsystem and the command-receiving subsystem (page 5, ¶1).

33. Apparatus for deterring failure of a computing system that is substantially exclusively made of substantially commercial, off-the-shelf components and that has at least one hardware subsystem for generating a response of the system to failure; said apparatus comprising (page 5, ¶1 "error signal collection"): a network of components having terminals for connection to such system (Figure 2); and circuits of the network

for operating programs to guard such system from failure (page 5, ¶1,2 "initiation of diagnosis"); the circuits comprising portions for reacting to said response of such hardware subsystem (page 5, ¶1).

34. The apparatus of claim 33, wherein: the reacting portions comprise sections for evaluating the hardware-subsystem response to establish characteristics of at least one recovery signal (page 5, ¶1).

35. The apparatus of claim 34, wherein: the reacting portions comprise sections for applying the at least one recovery signal to such system (page 5, ¶1).

36. The apparatus of claim 33, further comprising: such computing system, including such hardware subsystem (see above).

37. The apparatus of claim 33, particularly for use with a computing system that has plural generally parallel computing channels; and wherein (figure 2): the circuits comprise portions for comparing computational results from such parallel channels (page 5, ¶2 "voting").

38. The apparatus of claim 37, wherein: the parallel channels of the computing system are of diverse design or origin (page 5, ¶2 :"diverse M-nodes").

39. The apparatus of claim 33, particularly for use with a computing system that has plural processors (figure 2); and wherein: the circuits comprise portions for identifying failure of any of such processors and correcting for identified failure (page 5, ¶1:D-node functionality).

40. The apparatus of claim 33, wherein: the circuits comprise modules for collecting and responding to data received from at least one of the terminals, said modules comprising (page 5, ¶1: d-node functionality) : at least three data-collecting and -responding modules (page 5, ¶1: two or more), and processing sections for conferring among the modules to determine whether any of the modules has failed (page 5, ¶1 "voting").

41. The apparatus of claim 33, particularly for use with a computing system that is substantially exclusively made of substantially commercial, off-the-shelf components and that has at least one subsystem for generating a response of the system to failure, and that also has at least one subsystem for receiving recovery commands (page 5, ¶1); and wherein: the circuits comprise portions for interposing analysis and a corrective reaction between the response-generating subsystem and the command-receiving subsystem (page 5, ¶1).

42. Apparatus for deterring failure of a computing system that is distinct from the apparatus and that has plural generally parallel computing channels; said apparatus comprising (figure 2): a network of components having terminals for connection to such

system (figure 2); and circuits of the network for operating programs to guard such system from failure (page 5, ¶2); the circuits comprising portions for comparing computational results from such parallel channels (figure 2).

43. The apparatus of claim 42, wherein: the parallel channels of the computing system are of diverse design or origin (page 5, ¶2 "diverse M-nodes").

44. The apparatus of claim 42, wherein: the comparing portions comprise at least one section for analyzing discrepancies between the results from such parallel channels (page 5, ¶2 "voting").

45. The apparatus of claim 44, wherein: the comparing portions further comprise at least one section for imposing corrective action on such system in view of the analyzed discrepancies(page 5, ¶2 "replacement action").

46. The apparatus of claim 45, wherein: the at least one discrepancy-analyzing section uses a majority voting criterion for resolving discrepancies (page 5, ¶2 : "3 or more ... voting").

47. The apparatus of claim 42, further comprising: such computing system (see above).

48. The apparatus of claim 47, wherein: the parallel channels of the computing system are of diverse design or origin (see above).

52. The apparatus of claim 42, particularly for use with a computing system that has plural processors; and wherein: the circuits comprise portions for identifying failure of any of such processors and correcting for identified failure (page 5, ¶1).

53. The apparatus of claim 42, wherein: the circuits comprise modules for collecting and responding to data received from at least one of the terminals (page 5, ¶1, said modules comprising: at least three data-collecting and -responding modules (page 5, ¶1: two or more), and processing sections for conferring among the modules to determine whether any of the modules has failed (page 5, ¶2"voting").

54. The apparatus of claim 42, particularly for use with a computing system that is substantially exclusively made of substantially commercial, off-the-shelf components and that has at least one subsystem for generating a response of the system to failure, and that also has at least one subsystem for receiving recovery commands; and wherein (page 5, ¶1): the circuits comprise portions for interposing analysis and a corrective reaction between the response-generating subsystem and the command-receiving subsystem (page 5, ¶1).

55. Apparatus for deterring failure of a computing system that has plural processors; said apparatus comprising: a network of components having terminals for connection to such system (figure 2); and circuits of the network for operating programs to guard such system from failure(page 5, ¶1); the circuits comprising portions for identifying failure of any of such processors and correcting for identified failure (page 5, ¶1).

56. The apparatus of claim 55, wherein: the identifying portions comprise a section that corrects for the identified failure by taking a failed processor out of operation (page 5, ¶2 "replacement and safe shut down").

57. The apparatus of claim 56, wherein: the section comprises parts for taking a processor out of operation only in case of signals indicating that the processor has failed permanently (page 4, ¶9 describes removing only for permanent failures while page 4, ¶10-14 describe handling of transient failures removal is not disclosed for transient failures).

58. The apparatus of claim 55, wherein: the identifying portions comprise a section that substitutes and powers up a spare circuit for a processor taken out of operation (page 5, ¶2).

59. The apparatus of claim 55, further comprising: such computing system(see above).

60. The apparatus of claim 55, wherein: the circuits comprise modules for collecting and responding to data received from at least one of the terminals, said modules comprising (page 5, ¶1: d-nodes): at least three data-collecting and -responding modules (page 5, ¶1: "two or more"), and processing sections for conferring among the modules to determine whether any of the modules has failed (page 5, ¶1: "voting").

61. The apparatus of claim 55, particularly for use with a computing system that is substantially exclusively made of substantially commercial, off-the-shelf components and that has at least one subsystem for generating a response of the system to failure, and that also has at least one subsystem for receiving recovery commands page 5, ¶1); and wherein: the circuits comprise portions for interposing analysis and a corrective reaction between the response-generating subsystem and the command-receiving subsystem (page 5, ¶1).

62. Apparatus for deterring failure of a computing system; said apparatus comprising: a network of components having terminals for connection to such system (figure 2); and circuits of the network for operating programs to guard such system from failure (page 5, ¶1); the circuits comprising modules for collecting and responding to data received from at least one of the terminals(page 5, ¶1), said modules comprising: at least three data-collecting and -responding modules (page 5, ¶2), and processing sections for conferring among the modules to determine whether any of the modules has failed (page 5, ¶2).

63. The apparatus of claim 62, further comprising: such computing system (see above).

64. The apparatus of claim 62, particularly for use with a computing system that is substantially exclusively made of substantially commercial, off-the-shelf components and that has at least one subsystem for generating a response of the system to failure, and that also has at least one subsystem for receiving recovery commands (page 5, ¶1); and wherein: the circuits comprise portions for interposing analysis and a corrective reaction between the response-generating subsystem and the command-receiving subsystem (page 5, ¶1).

65. Apparatus for deterring failure of a computing system that is substantially exclusively made of substantially commercial, off-the-shelf components and that has at least one subsystem for generating a response of the system to failure, and that also has at least one subsystem for receiving recovery command (page 5, ¶1)s; said apparatus comprising: a network of components having terminals for connection to such system between the response-generating subsystem and the recovery-command-receiving subsystem (page 5, ¶2); and circuits of the network for operating programs to guard such system from failure)(page 5, ¶1); the circuits comprising portions for interposing analysis and a corrective reaction between the response-generating subsystem and the command-receiving subsystem (page 5, ¶2).

66. The apparatus of claim 62, further comprising: such computing system (see above).

Allowable Matter

Claims objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicant is reminded the claims are indicated as allowable as a whole including any intervening base claims.

49. The apparatus of claim 48, wherein: the comparing portions comprise circuitry for performing an algorithm to validate a match that is inexact.

50. The apparatus of claim 49, wherein: the algorithm-performing circuitry employs a degree of inexactness suited to a type of computation under comparison.

51. The apparatus of claim 49, wherein: the algorithm-performing circuitry performs an algorithm that selects a degree of inexactness based on type of computation under comparison.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bryce P Bonzo whose telephone number is (703) 305-4834. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Bryce P. Bonzo

Bryce P Bonzo
Examiner
Art Unit 2114

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